

FIG. 1 is a block diagram of a phase-locked loop (PLL) circuit 10, which is used to generate a 19.44 MHz signal from a 19.44 MHz local oscillator signal.

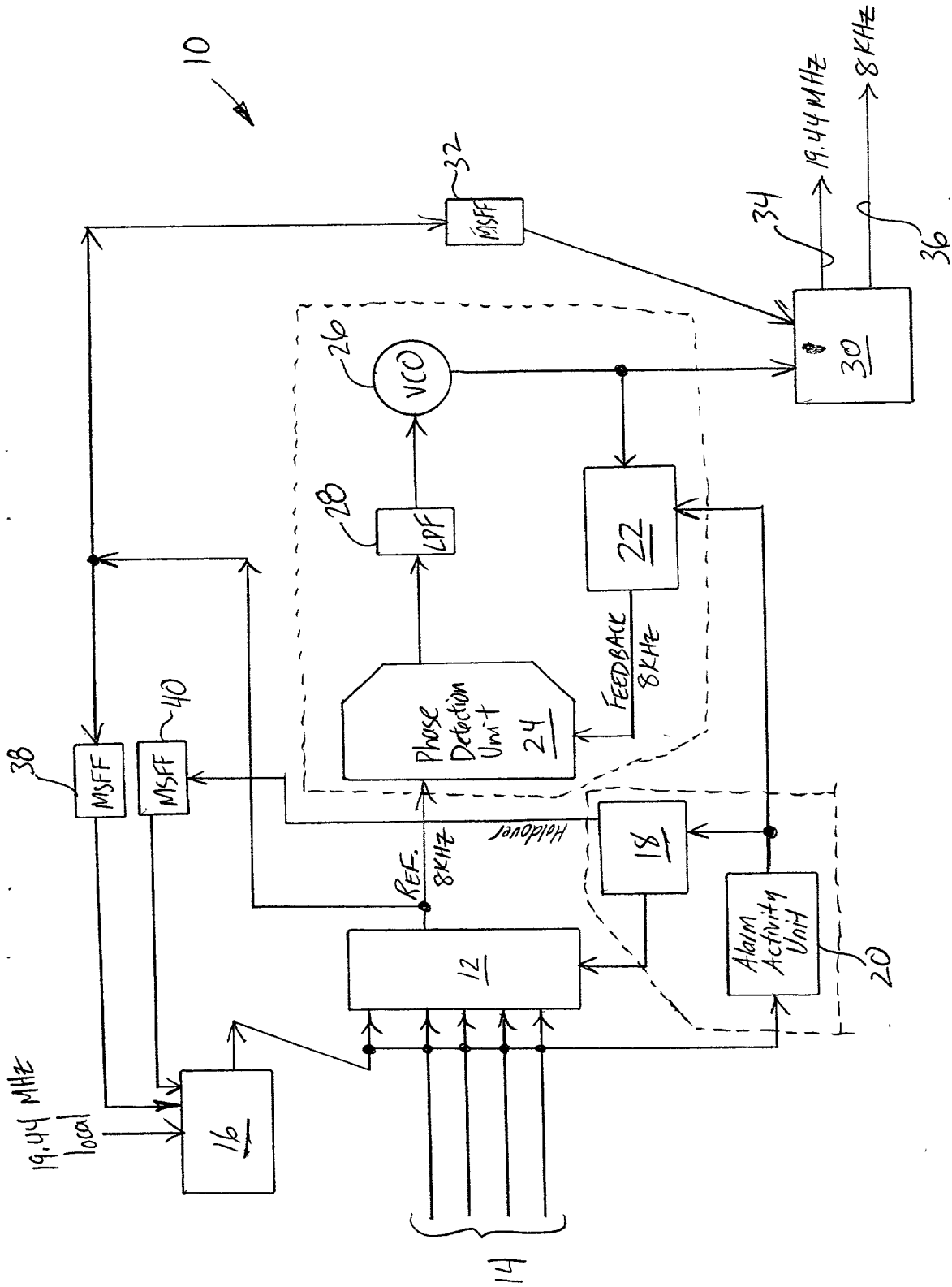
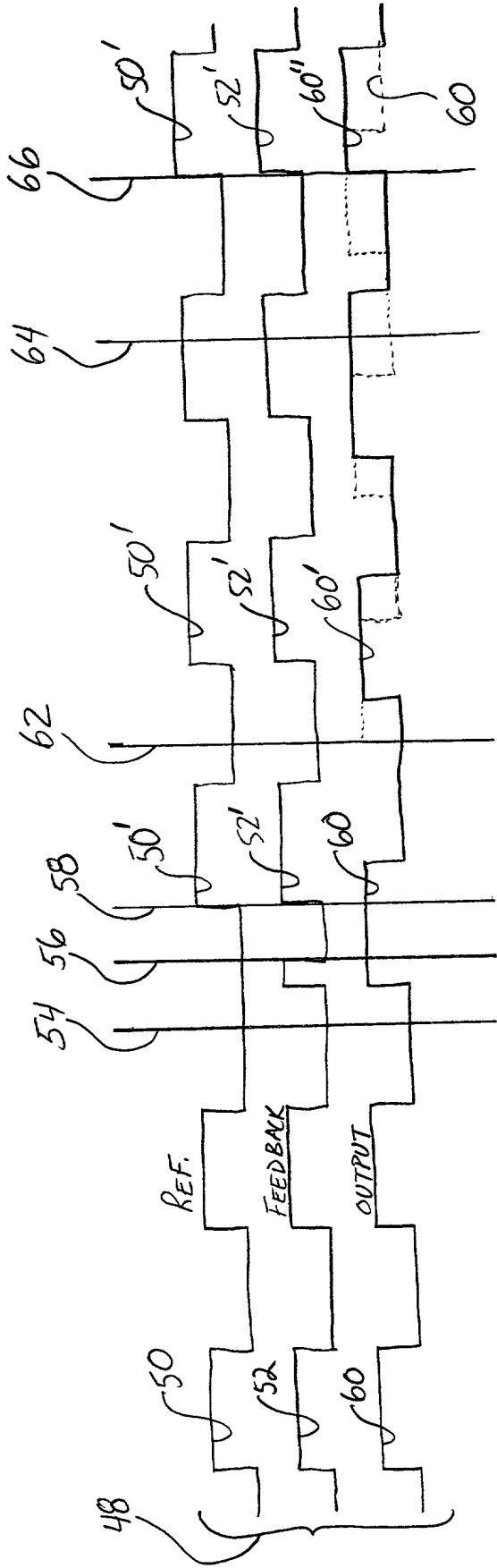


Fig. 1

Hand-drawn schematic diagram of a control system showing REF, FEEDBACK, and OUTPUT signals. The diagram includes various components labeled 48, 50, 52, 60, 54, 56, 58, 62, 64, and 66. The signals are represented by step functions. The REF signal is a single pulse. The FEEDBACK signal is a series of pulses. The OUTPUT signal is a series of pulses. The diagram is labeled with various numbers and letters, including 48, 50, 52, 60, 54, 56, 58, 62, 64, and 66. The signals are represented by step functions. The REF signal is a single pulse. The FEEDBACK signal is a series of pulses. The OUTPUT signal is a series of pulses. The diagram is labeled with various numbers and letters, including 48, 50, 52, 60, 54, 56, 58, 62, 64, and 66.



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Fig. 2

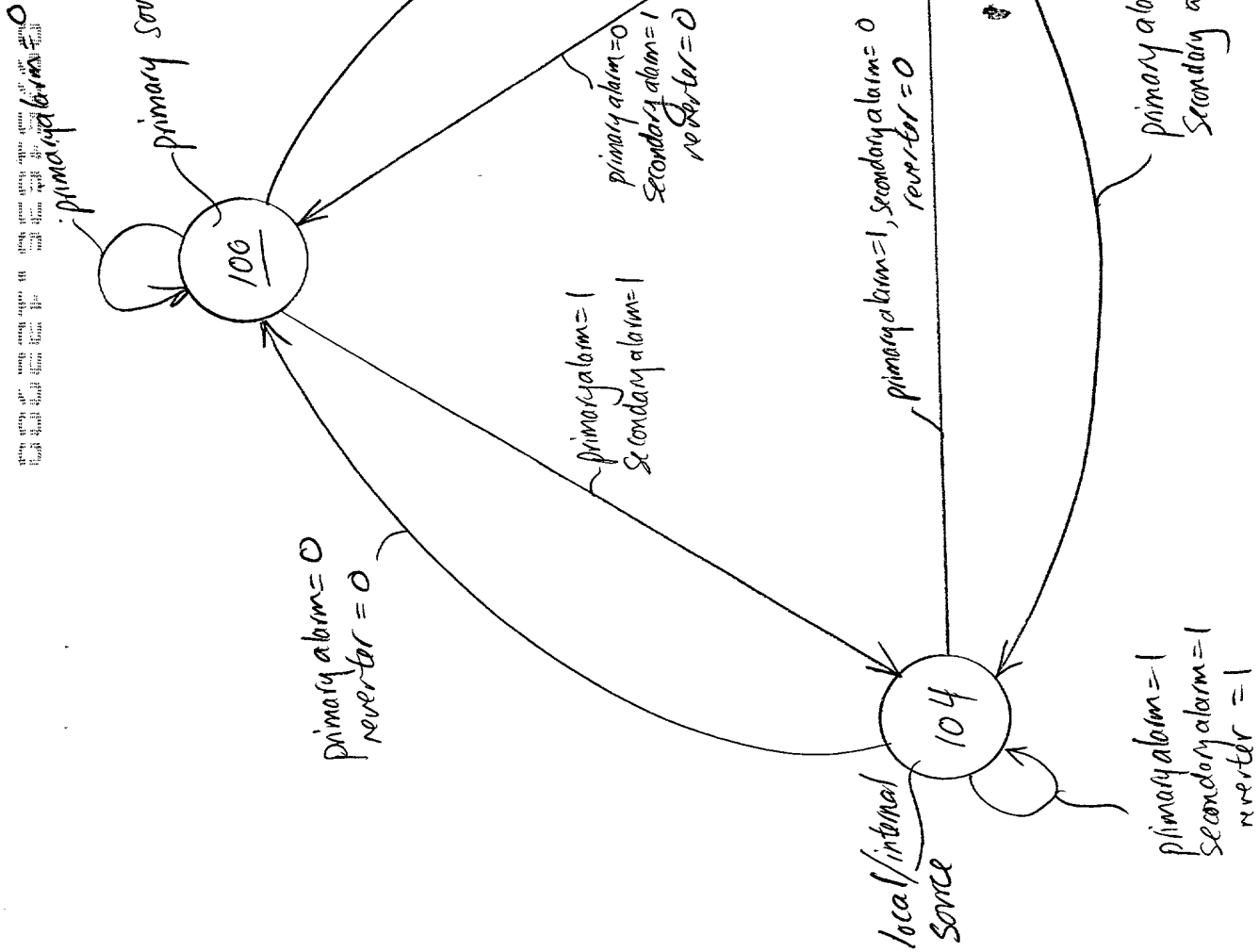


Fig. 3